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ORIGINAL PAPER

# Developing a parametric carbon footprinting tool for the semiconductor industry

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**Abstract** The advent of global awareness of sustainable development resulted in consumer demand for low-carbon electronic products. Thus, semiconductor industry has to develop additional core competencies in that direction to remain competitive. The present study aims to establish a parametric-based tool that can identify key parameters of the complicated manufacturing processes in the semiconductor industry to simplify the calculation of the carbon footprint of products (CFP). Six regression models for CFP were developed by applying process and statistical analyses on 7114 wafer products. Results indicate that these regression models with the three key parameters (mask layer, metal layer, and technology node) can effectively predict the CFP of wafer with six different function types because the adjusted $R^2$ of all regression models was >0.5. Moreover, the mask layer could be the most important parameter for predicting CFP of wafer because of its higher standardized coefficients ($\beta$) in each regression model. This methodology reduces the time, cost, and information requirements of the product in traditional life cycle assessment. The proposed method introduces criteria for low-carbon decision making in the semiconductor sector.

**Keywords** Low-carbon design · Parametric carbon footprinting · Regression analysis · Semiconductor manufacturing · Green competitiveness

## Introduction

Climate change has become a major issue after the publication of several scientific studies, particularly studies by the Intergovernmental Panel on Climate Change (IPCC). Climate change significantly affects the earth and human systems, such as ecosystems, water resources, food security, and health (IPCC 2007). Economies must decouple environmental impacts from development processes, and policy formulation is increasingly turning to the "green economy" to simultaneously meet the challenges from the economic downturn, thereby addressing climate change issues (Potts 2010). Numerous countries have implemented various regulations or directives to make their economies more green and environment-friendly (Digas et al. 2014). Similarly, products and services are subject to strict evaluation in terms of its environmental impact (Kolk and Pinkse 2004; Hsu and Hu 2008). Ultimately, the demand for green products and services will increase, along with the pressure to reduce greenhouse gas (GHG) emissions and to disclose data on environmental impact, such as carbon footprints (Wang and Chiu 2014). For a long time, the primary competitive edge of the semiconductor industry has been its speed, cost, flexibility, and quality (Chang and Tsai 2002; Wu et al. 2006). However, the increasing global awareness of sustainable development resulted in the need for the development of low-carbon electronic products. The semiconductor industry should develop additional core competencies in that direction. For

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example, GHG emissions should be disclosed, and efforts should be made to mitigate such emissions (Hsu et al. 2014).

Over the past few years, carbon footprint has become one of the most important indicators of environmental protection (Wiedmann and Minx 2008; Lam et al. 2010; Galli et al. 2012). Carbon footprint is usually quantified as global warming potential (GWP), which represents the quantities of GHGs that contribute to global warming and climate change. Given that the environmental impact of semiconductors is crucial to the assessment of electronic products, researchers have investigated the carbon footprint of the semiconductor manufacturing industry. Murphy et al. (2003) developed parametric unit operation modules to estimate material requirements, energy requirements, and emissions in wafer fabrication. This method can be used for carbon footprinting. Higgs et al. (2009) developed an overall carbon footprinting for the relative $CO_2$ impacts of the various aspects of semiconductor production and use, including manufacturing operations, product use, and various scope 3 impacts (i.e., supply chain, logistics, and employee travel). Boyd et al. (2009, 2010) developed a life cycle energy analysis for complementary metal–oxide–semiconductor and digital logic chips over seven technology nodes to compare energy demand and GWP impacts of the life cycle stages, respectively. Liu et al. (2010) selected two life cycle assessment (LCA) methods to evaluate the GWP from direct/indirect $CO_2$ emissions and energy consumption of production equipment, which are the major environmental impacts of dynamic random access memory products. Higgs et al. (2010) focused on the energy and $CO_2$ impacts associated with the creation of high-purity-grade materials that are required for semiconductor manufacturing. In the integrated circuit (IC) packaging technologies, Andrae and Andersen (2011) studied the change in GWP100 and Eco-Indicator 99 (H) scores on component and printed circuit board assembly levels when traditional component packaging is replaced with nanostructured polymer particles.

At present, the two main limitations in performing carbon footprinting are the required time and expertise and the lack of uniformity and integrated platform (Meinrenken et al. 2012). Although PAS 2050 (BSI 2011) and the latest ISO/TS 14067 (ISO 2013) have helped develop carbon footprint of product (CFP) as a sub-discipline of LCA, performing CFP of IC is often unattainable because of the relatively short development cycle and rapid change in design and manufacturing technologies. Thus, the assessment of existing chips has become obsolete in a few years (Harland et al. 2008; Boyd 2012). The manufacturing process of semiconductors from upstream to downstream of the value chain is composed of four phases, they are as follows: IC design, wafer fabrication, IC test, and IC packaging (Wang and Chiu 2014). In wafer fabrication, hundreds of machines operate together under various constraints and procedures to construct multiple layers of chemical patterns on a silicon wafer (Kumar 1994; Mason et al. 2002). The initial layers after release are basic operations for all types of wafers, and several layers, including poly and metal operations, can be distinctly identified based on product specification (Chung et al. 2008). Every layer should be processed in a similar manner. Thus, the wafers should be processed by a particular machine several times, one layer of circuitry at a time. This process is known as the reentrant product flow (Toktay and Uzsoy 1998). In addition, wafer fabrication is characterized by hybrid machine types as well. Several types of equipment operate simultaneously in wafer fabrication (Guo et al. 2012). Furthermore, the semiconductor industry is a complex network comprising firms that specialize in specific stages of the semiconductor manufacturing process. Nevertheless, the considerable amount of data and the lack of specific system boundaries have resulted in increasingly difficult assessments for a practitioner to conduct CFP. Hence, the semiconductor industry should develop a simple and efficient method for assessing CFP.

In recent years, several studies on fast carbon footprinting have been published (Song and Lee 2010; Meinrenken et al. 2012; Kuo 2013). Findings from these studies resulted in the construction of a collaborative system to help enterprises collect and calculate CFP in a readily and timely approach by integrating the enterprises' internal data from the enterprise resource planning system or similar data warehouses, such as the bill of materials (BOMs). The major steps are as follows: establishing the GHG emission target and the BOM structure, forming the GHG BOM, estimating the GHG emissions of the product, identifying problematic parts, selecting alternative parts, and evaluating the GHG emissions of the newly designed product. Thus, the alternative parts for the design of a low-carbon product were easily and quickly evaluated in the above-mentioned studies. Some researchers have proposed methodologies to achieve fast carbon footprinting in the semiconductor industry. Boyd et al. (2006) designed a tractable, parametric, and secure structure to evaluate energy use, material input, and emissions data, such as carbon footprint, to comparatively assess the environmental implications of semiconductor fabrication. Dessouky et al. (2011) proposed a user-friendly carbon footprint model to promote student awareness of the effect that changes in manufacturing technologies and transportation modes could have on the carbon footprint of the semiconductor industry's supply chain. Villard et al. (2012) developed an eco-design tool for semiconductor manufacturers. This tool equipped the designers with basic environmental knowledge during the analysis phase while

ensuring the microchips' high environmental performance. Such findings could be used to predict changes in inventory resulting from the changes in semiconductor product design by integrating the materials and energy consumption and carbon emission at each unit of the manufacturing process. Results have shown that looping the same algorithm could reduce the enterprises' investment in man power and resources for carbon footprint inventories and could allow for the footprinting of all products and services, but these algorithms are not easily obtained and applied by companies because of BOMs or the confidentiality of the internal data of other enterprises. Therefore, this approach is suitable for use by a company that is capable of a full in-house production (i.e., from the design stage to the manufacturing stage). However, this approach cannot be applied to some semiconductor companies because of its specialized production divisions, such as Media Tek in fabless IC supply (design stage) and Taiwan Semiconductor Manufacturing Company (TSMC), and United Microelectronics Corporation (UMC) in pure-play IC foundry (manufacturing stage). Hence, the primary purpose of this study was to develop a fast carbon footprinting tool based on common language (i.e., customer order factors and parameters of critical manufacturing processes) in the semiconductor industry instead of BOMs or internal data from other enterprises. The customer order factors are the specifications of IC products, such as function type, technology node, and mask layer, required from customers. The proposed model can be validated through its application in distinct companies in the semiconductor industry from upstream to downstream. Moreover, carbon emission at the different stages of a supply chain can present a significant threat that requires careful attention during the design phase of the supply chain (Sundarakani et al. 2010). Thus, a carbon footprinting tool has to be established for the supply chain of the semiconductor industry, particularly at the wafer design stage. The tool should be able to readily evaluate each wafer's carbon footprint, which serves as a guide for the development of a low-carbon product design.

The present study is a part of a larger European Union project—Boosting Life Cycle Assessment Use in SMEs: Development of Sectoral Methods and Tools (LCA to go)—which is funded by the Seventh Research Framework Program. This study aims to simplify CFP calculation by establishing a parametric-based tool that can identify the key factors of the complex manufacturing processes in the semiconductor industry. This paper is organized as follows: the next section describes the research materials and methods for developing a parametric carbon footprinting tool; the penultimate section presents general findings from the results and limitations of this study; and the final section summarizes key conclusions and industry implications. The analytical data of this study were collected from eight semiconductor factories in Taiwan from 2010 to 2011.

## Materials and methods

### Research procedure

The three steps in developing a parametric carbon footprinting tool are as follows:

*Step 1: key parameters are identified*

All possible parameters were selected based on the customer order in the design stage and the critical wafer fabrication manufacturing processes, such as technology node and mask layer. The selection of the parameters was based on the literature review and industry experience in semiconductor manufacturing. Process and correlation analyses were applied to identify key parameters. Process analysis was used to investigate the relationship between altering parameters and energy and material consumption to assess the effect of the processes on CFP. Correlation analysis was used to assess the strength of the relationship between two variables, namely parameters and CFP. Correlation analysis was based on a correlation coefficient, Pearson's $r$.

*Step 2: the parametric tool is developed*

In this step, the relationship between carbon emissions and selected parameters during the processes of wafer fabrication were examined using regression analysis. In statistics, regression analysis helps elucidate the changes in the dependent variable's typical value when any of the independent variables is varied. The other independent variables are fixed. In the present study, regression analysis was applied to establish regression models using the key parameter for predicting the CFP of wafer fabrication.

*Step 3: the proposed parametric tool is calibrated*

To maintain consistency in data on the enterprises at different geographical locations or technical levels, the proposed tool considered the carbon emission factor of electricity and OWE in different enterprises.

### System boundary and scope

The system boundary of the study in terms of the IC product's life cycle was set to include only the front-end wafer processes and not the entire life cycle. The stages involving the testing of IC and the use and disposal of electronic

equipment and facilities were excluded from the analysis. The method used for the simplified semiconductor CFP approach follows the IC Product Category Rules (PCR) of the Environmental Product Declaration (TSMC et al. 2009), which can be used to assess the environmental impacts on global warming, acidification, ozone depletion, photochemical oxidant formation, eutrophication, water, and energy. This study focuses on global warming (kg $CO_2$ equivalent) as the environmental impact. The LCA includes information for the following unit processes: material extraction and production for main materials and their raw materials, manufacturing of main auxiliary materials, and manufacturing and assembly of product and transportation of materials and products. Auxiliary materials mean the materials will be used in the manufacturing process, but will not contain in the product. Details are shown in Fig. 1.

## Functional unit

The functional unit for the wafer is defined per wafer [e.g., 150 mm (6 in), 200 mm (8 in), or 300 mm (12 in) wafer] according to IC PCR (TSMC et al. 2009). All energy and materials, such as perfluorinated compound (PFC) emissions, electricity usage, water usage, waste treatment, and sewage disposal discharge, were calculated into the system at each step of the process. The consumption of each equipment moving in the process was considered in this study.

## Data collection and assumptions

The inventory data of carbon emissions for various products (wafers) were collected from eight semiconductor factories in Taiwan. All inventory data were collected from 2010 to 2011 in accordance with the rules of PAS 2050 and IC PCR (BSI 2011; TSMC et al. 2009). The data collection was a lengthy process, and the data sources were based on enterprise resource planning system, which integrates all facets of an operation, including general information on product and processing equipment, data sheets for energy and materials, and GHG inventory. To investigate the relationship between processes and $CO_2$ emission with different wafer characteristics, UMC developed a method for calculating the CFP of wafer products (Yin et al. 2013). This method is based on IC PCR and is used to perform an inventory of the carbon footprint of the entire factory. Subsequently, this method is used to allocate data into different products by each "move" of the process. The inventory item of the entire factory includes the consumptions of materials related to wafer fabrication, GHG emissions of PFC, energy consumptions of manufacturing processes and factories, and information on waste treatment. The manufacturing process of wafer fabrication is not a straight-line production process, but rather a procedure composed of many repeated sequential processes. Passing the same equipment many times is possible. Hence, the definition of "move" is the number of times that each process equipment passes during the entire manufacturing process of the product. "Moves" include the moves of diffusion, etch, thin film, and photo equipment. By performing the above-mentioned method, this study can allocate the consumptions of energy and materials to each product by its moves and consequently calculate the CFP of different product specifications. Some assumptions are made based on interviews with engineers of IC plants. The number of major equipment is used as a benchmark to allocate the consumption of total electricity and energy and chemicals, such as photoresistive liquids, slurries, and developers. In addition, this study uses the

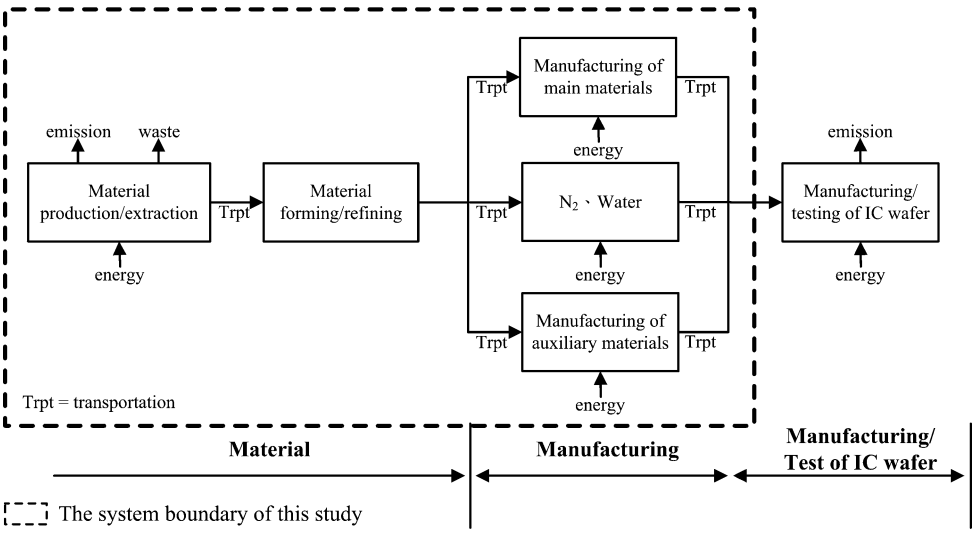


**Fig. 1** System boundary and scope of IC front-end wafer processes. Reference: modified from IC PCR (TSMC et al. 2009)

information from material safety data sheets (MSDS) to calculate the mass and weight proportion using the mass balance obtained from chemical equations.

## Results and discussion

### Data description

This study conducted CFP for the fabrication of a total of 7114 products through six parameters, namely function type, generation, technology node, mask layer, metal layer, and poly layer. The function types of the wafers are classified into six categories based on their process technologies and general purpose (Hu et al. 2013a), they are as follows: CMOS Image Sensor (CIS), embedded high voltage (eHV), embedded nonvolatile memory (eNVM), logic/mixed signal (Logic/MS), power management IC (PMIC), and other function types. The generations of products include 6, 8, and 12 in wafers. Technology node is defined as the rules of a process that are governed by the smallest feature printed on a repetitive array. Mask layer is an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. Mask layers are commonly used in photolithography, and the quantity of such layers represents the level of complexity of the wafer (Taiariol et al. 2001; Yao et al. 2004). Metal layer is used to improve the stability of different layers on the wafer. Moreover, capacitors can be created by stacking different metal layers. The poly layer is essential for semiconductor processing and can be used for protecting the metal layer from melting at high temperature.

### Identify key parameters

In this step, process and correlation analyses were applied to identify the key parameters for CFP of wafer fabrication and to investigate the relationship between parameters and $CO_2$ emission. The process analyses have two objectives: to understand the situation of the effect of the parameters on application of IC, and to investigate the relationship between the parameters and energy and material consumption to assess the effect of the processes on CFP. Moreover, correlation analysis was conducted to measure the strength of the relationship between the parameters and CFP based on the 7114 products. For the generation, the correlation analysis results showed that wafer generation will affect CFP. In contrast, different generations of wafers will primarily affect the number of dies that could be divided but not the application of IC. Moreover, the wafer generations often vary across distinct semiconductor companies for each function type. Hence, generation was not considered a key parameter for predicting CFP of wafer fabrication. To examine the relationship between alterations in parameters and CFP in a single-function type, this study integrated three different generations of wafer to increase the analytical data in single-function type; the functional unit was redefined as per $mm^2$ of wafer in the next step. For the technology node, the complexity of the device design increased, thereby increasing the number of procedures required to produce a finished wafer. Thus, as technology node decreases, the process difficulty increases, thereby increasing the consumption of energy and material. The correlation analysis results also showed that technology node will affect CFP. On the one hand, for the mask layer, the manufacturing processes of the mask layer contain most of the processes in wafer fabrication, and each layer is created from different masks and materials. On the other hand, the increase in the quantity of mask layers and the consumption of energy and material will affect the wafer's CFP. This finding corresponds with the results of correlation analysis. For the metal layer, most PFC emissions emanate from the processing of the metal layer (IPCC 2001). This finding means that the quantity of metal layers increased, thereby increasing the carbon emissions of wafer. The correlation analysis also found that the quantity of metal layers on wafer affects CFP. This finding indicates that the technology node, mask layer, and metal layer were not only essential parameters in the design stage of wafer but also important factors that affect CFP. Therefore, these three parameters were considered the key parameters. Although the poly layer was also an essential parameter in the wafer design stage, the quantity of poly layers on wafer did not affect CFP in the results of process analysis with energy and material consumption and correlation analyses. This finding is likely caused by the fact that the range of poly layer is narrow (i.e., the quantity of poly layers does not differ significantly from different wafers). Thus, the poly layer was removed from this step. The details of the determination of key parameters are shown in Table 1.

### Development of the parametric tool

After identifying the key parameters, this study planned to apply regression analysis to establish regression models using these three key parameters for predicting the CFP of wafer with different function types. To apply regression analysis, the analytical data of 7114 products were classified according to their function type, and then, the quantity of the three key parameters was listed in each analytical data. The unit of technology node was unified into μm. The CFP of each analytical datum was redefined as per $mm^2$ of wafer in the previous step. This study selected these three parameters as independent variables and the CFP as the

**Table 1** Determination of the key parameters

| Parameters | Process analysis with | | Correlation analysis with CFP | Implication |
|---|---|---|---|---|
| | Application of IC | Energy and material consumption | | |
| Generation | Weak relationship | Strong relationship | High positive ($r = 0.847 > 0.5$) | Identified as not a key parameter |
| Technology node | Strong relationship | Strong relationship | High negative ($r = -0.501 < -0.5$) | Identified as a key parameter |
| Mask layer | Strong relationship | Strong relationship | High positive ($r = 0.676 > 0.5$) | Identify as the key parameter |
| Metal layer | Strong relationship | Strong relationship | High positive ($r = 0.735 > 0.5$) | Identify as the key parameter |
| Poly layer | Strong relationship | Weak relationship | Low positive ($r = 0.182 < 0.5$) | Identified as not a key parameter |

**Table 2** Data for applying regression analysis

| Product no. | Function type | Key parameters | | | CFP[a] g $CO_2$ e/$mm^2$ |
|---|---|---|---|---|---|
| | | Technology node (μm) | Mask layer | Metal layer | |
| 1 | CIS | 0.35 | 20 | 1 | – |
| 2 | CIS | 0.18 | 25 | 2 | – |
| 3 | eNVM | 0.18 | 25 | 3 | – |
| 4 | PMIC | 0.28 | 30 | 5 | – |
| ~ | ~ | ~ | ~ | ~ | ~ |
| 7114 | eHV | 0.35 | 40 | 7 | – |

[a] The CFP of products were not disclosed due to confidentiality

dependent variable to apply regression analysis to establish six regression models with different function types. Details of the analytical data are shown in Table 2.

Before establishing the regression models, the interaction of the variables in these regression models should be investigated by collinearity diagnostics to understand the situation of multicollinearity. Multicollinearity refers to the presence of highly intercorrelated predictor variables in regression models, and its effect is to invalidate some basic assumptions underlying their mathematical estimation. Collinearity diagnostics measure the extent of the relationship between regressors and other regressors, and how this relationship affects the stability and variance of the regression estimates. This study applied the collinearity diagnostics by assessing the tolerances, variance inflation factor (VIF), and condition indices (CI) of these regression models (Coenders and Saez 2000). The results indicated that the tolerances were <0.1, the VIFs were >10, and the CIs were >30 for all variables of these regression models (Table 3). In other words, multicollinearity did not exist in these regression models. The simplified CFP equation for wafer fabrication in the semiconductor industry is expressed as

$$\begin{aligned}&\text{CFP of } \text{mm}^2 \text{ wafer with } A_i \text{ function type}\\ &\quad = \alpha_1 + \alpha_2 \times \text{Technology node}\\ &\qquad + \alpha_3 \times \text{Mask layers} + \alpha_4 \times \text{Metal layers}\end{aligned} \tag{1}$$

where CFP denotes the carbon footprint per $mm^2$ of wafer with $A_i$ function type, which included six different function types. The different $\alpha_j$ were constants, which depend on the selection of function type. Thus, this equation could be used to predict the CFP of wafer by inputting the quantity of the three key parameters. The results could likewise be applied to different generations of wafer. In contrast, the CFP of 6, 8, and 12 in wafers could be obtained by multiplying their sizes.

It is commonly used in applied statistics to evaluate inferences based on their statistical significance at the 5 % level (Gelman and Stern 2006). Therefore, $p$ value <0.05 was considered to be statistically significant in this study. The results show that the three key parameters, namely mask layer, metal layer, and technology node, affected CFP because these parameters were significant at $p$ values <0.001 in each regression model. In statistics, the coefficient of determination ($R^2$) is a statistical measure of how well the regression line approximates the actual

**Table 3** Details of the regression models

| Function type | Standardized coefficients ($\beta$) | | | Collinearity diagnostics | | | $R^2$ | Adjusted $R^2$ |
|---|---|---|---|---|---|---|---|---|
| | Technology node | Mask layer | Metal layer | Tolerance | VIF | CI | | |
| CIS | 0.26*** | 0.82*** | 0.42*** | 0.54–0.90 | 1.11–1.85 | 4.64–19.69 | 0.80 | 0.79 |
| eHV | 0.17*** | 0.72*** | 0.10*** | 0.30–0.45 | 2.47–3.36 | 2.89–14.54 | 0.50 | 0.50 |
| eNVM | 0.05*** | 0.69*** | 0.30*** | 0.17–0.35 | 2.88–6.07 | 3.17–20.66 | 0.85 | 0.85 |
| Logic/MS | 0.06*** | 0.56*** | 0.27*** | 0.24–0.44 | 2.25–4.53 | 2.82–17.09 | 0.58 | 0.58 |
| PMIC | 0.03*** | 0.68*** | 0.29*** | 0.21–0.98 | 1.02–4.82 | 2.79–11.18 | 0.89 | 0.89 |
| Other | 0.23*** | 0.90*** | – | 0.93, 0.93 | 1.08, 1.08 | 4.06–10.66 | 0.76 | 0.74 |

*** $p < 0.001$

observations. An $R^2$ of 1 indicates that the regression line perfectly fits the data. However, as the number of fitted coefficients in the regression model increases, $R^2$ will increase although the fit may not improve in a practical sense (Mittlböck 2002). Thus, this study used the adjusted $R^2$ that considers the degrees of freedom to avoid this situation. The results indicated that the adjusted $R^2$ of all regression models was >0.5; some of them were even >0.85. This finding means that these regression models with key parameters can effectively predict the CFP of wafer fabrication. Moreover, these regression models can be applied to the six different function types of wafer, namely CIS, eHV, eNVM, Logic/MS, PMIC, and other function types. It is found that the regression models of CIS, eNVM, PMIC, and other function types were more effective in predicting CFP than that of eHV and Logic/MS function types. This finding is likely caused by the fact that the classification of the eHV and Logic/MS function types was more varied than the other function types. As such, not all product characteristics could be covered even if this study classified the products based on their process technologies and purpose. For example, the eHV function type may include double-diffused drain metal–oxide–semiconductor field-effect transistors (MOSFET), field drift MOSFET, and other types. Moreover, technology nodes range from 0.8 μm to 55 nm. Thus, the $R^2$ of this regression model may be affected. Furthermore, the mask layer could be the most important parameter for predicting CFP because of its higher standardized coefficients ($\beta$) in each regression model. Details of these regression models are shown in Table 3.

## Calibrating the parametric tool

To obtain the best prediction results, the proposed tool considered the carbon emission factor of electricity and OWE in different enterprises, which are described in detail below.

### *Carbon emission factor of electricity*

Using data from the Taiwan Power Company, electricity usage in Taiwan was inventoried through LCA. Regarding the 7114 products, the average carbon emission of electricity usage accounted for 60 % of CFP. Hence, the carbon emission factors of electricity can be adjusted using the proposed tool. For example, when a researcher applies Eq. (1) to obtain the CFP of wafer with a certain function type, then the CFP will contain 60 % of carbon emissions from electricity usage. Therefore, the amount of electricity (kWh) could be calculated in this study by dividing the carbon emission factor of electricity. In this way, a researcher can exchange the 60 % of carbon emissions by multiplying other carbon emission factors of electricity according to different scenarios.

### *Overall wafer effectiveness*

OWE refers to the fraction of good die area to total wafer area (Chien et al. 2013). The useful wafer area, which is the product of the number of good die and die size, is determined using yield rate and gross die number. For example, when a researcher applies Eq. (1) to obtain the CFP of wafer with a certain function type, the CFP as pieces of die could be obtained by dividing by the number of good dies based on the technical levels of different enterprises. As such, combining the IC back-end processes, IC test, and IC packaging to integrate the CFP of the entire semiconductor manufacturing process would be easier (Hu et al. 2012). The methodology for back-end processes is still under development. Currently, the body size of package and usage of wire are identified as the key parameters for predicting the CFP of back-end processes (Hu et al. 2013b).

To clearly demonstrate the application of this study, a simulated CFP calculator for wafer fabrication was created based on these regression models. The operation steps are

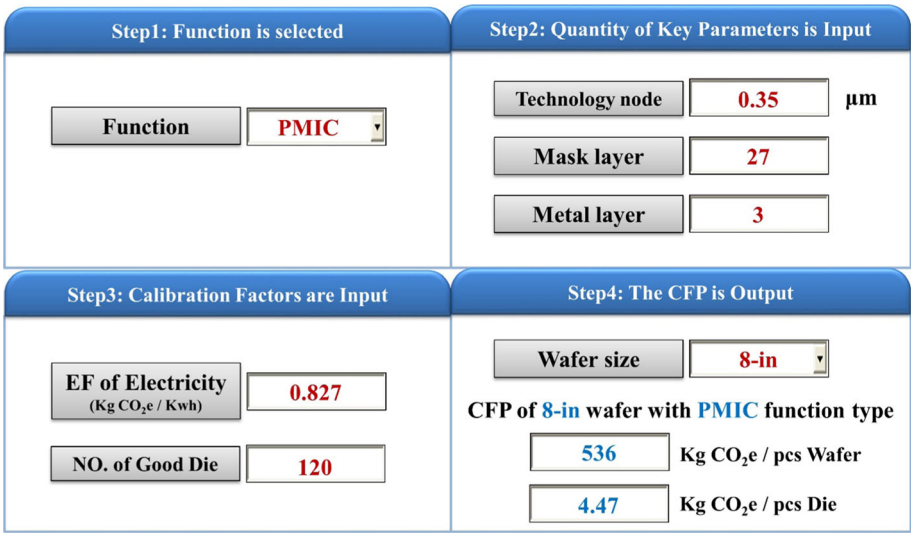


**Fig. 2** Simulated CFP calculator for the semiconductor industry. *Note* data in this figure are examples, not actual data

as follows: First, the function is selected. Six functions are included in this simulated CFP calculator, namely CIS, eHV, eNVM, Logic/MM, PMIC, and other function types. These functions can be selected according to their general purpose. Second, the quantity of key parameters can be input to predict the CFP. Third, the calibration factors are inputted. The carbon emission factor of electricity and the number of good dies to calibrate the difference in enterprises must be inputted. Finally, the simulated CFP calculator will output two types of CFP, such as pcs wafer and pcs die, according to the choice of wafer size. Details are shown in Fig. 2.

## Discussion and limitations

In this paper, a parametric carbon footprinting tool for wafer fabrication in the semiconductor industry was developed. The presented methodology reduced the time, cost, and information requirements of the product for traditional LCA, as well as provided criteria for low-carbon design by adjusting the quantity of key parameters. Moreover, the calibration factors (i.e., carbon emission factor of electricity and OWE) can be adjusted in the proposed parametric carbon footprinting tool to strengthen the application. Although several fast carbon footprinting approaches for the semiconductor industry have been proposed in previous studies (Boyd et al. 2006; Dessouky et al. 2011; Villard et al. 2012), which integrated material and energy consumption with carbon emission at each equipment unit of the manufacturing process, these approaches are suitable for use by a semiconductor company that is capable of completely in-house production, from design to the manufacturing stage. However, this approach may be inapplicable to some semiconductor companies that have separate design and manufacturing stages due to the confidentiality of this internal information of other enterprises. This study identified three key parameters, namely mask layer, metal layer, and technology node, which should be able to improve the current carbon footprinting practice in semiconductor industry, because these parameters are external product specifications, and their quantity is part of the customer order in the IC design stage.

The three key parameters of this study correspond with those reported in previous studies. For the mask layer, the pattern is "stepped" or repeated many times across the wafer to produce multiple dies. A single mask layer involved four unit operations (i.e., wafer clean, furnace, photolithography, and etch) and seven processes (i.e., particulate removal, film deposition, resist coat, resist expose, resist develop, film patterning, and resist removal; Murphy et al. 2003), that is, the manufacturing processes of the mask layer contain most of the processes in wafer fabrication. The quantity of mask layers represents the level of complexity for wafer (Taiariol et al. 2001; Yao et al. 2004). Boyd et al. (2006) implemented life cycle inventory for a comparison between a six-layer wafer and an eight-layer wafer with the same specifications. The results indicated that the increase in the quantity of layers and the consumption of energy and material will affect the wafer's CFP. For the metal layer, PFCs are used for both plasma cleaning of chemical vapor deposition chambers and plasma (dry) etching of thin insulating and metal layers (IPCC 2001). This situation means that the quantity of metal layers increased, thereby increasing the carbon emissions of wafer. For the technology node, Boyd et al. (2009) reported that as technology node progressed, life cycle energy use and GHG emissions increased per wafer. At each technology node, the complexity of the device design increased, thereby increasing the number of procedures required to produce a finished wafer. In summary,

each of these three key parameters was closely related with the CFP of the wafer. Therefore, the parametric carbon footprinting tool could enhance the accuracy of prediction results for CFP when simultaneously considering the three key parameters.

This study has several limitations. First, semiconductor companies that engage in pure-play IC foundry can apply the key parameters to examine the relationship between carbon emissions and the process of wafer fabrication, and establish their own regression models to increase the prediction results in the design stage. However, these companies should finalize CFP calculation before developing their own parametric tools. Calculating CFP may not be a considerable problem because several life cycle inventory approaches for semiconductor manufacturing have been proposed in previous studies (Murphy et al. 2003; Boyd et al. 2006, 2009). Second, the parametric tool proposed in this study can be applied to six different wafer function types. However, this tool cannot cover all product characteristics even if this study classified them based on their process technologies and general purpose. To strengthen the application, a comprehensive wafer classification approach should be established in future studies. Finally, the system boundary of the study has been set to include only the cradle-to-gate process and not the entire life cycle. However, the main source of carbon emissions for semiconductor products is the stage of IC usage in electronic products (Boyd et al. 2009, 2010). Therefore, some parameters in the usage of common electronic products should be incorporated in this parametric tool.

## Conclusion

Although climate change issues can be considered a threat, others regard them as an opportunity (Lash and Wellington 2007). The semiconductor industry should respond to this direction and develop core competencies that are environmentally friendly to remain competitive and sustainable. The carbon footprint per IC has been defined as the early IC design stage. Thus, enterprises at the design stage should have timely disclosure of CFP from the manufacturing stage to set the criteria for low-carbon decision making. Moreover, the applicability of confidential and exclusive information by companies should be considered when characterizing the specialized production division in the semiconductor industry. This study proposed a parametric carbon footprinting tool that is suitable for the aforementioned features in the semiconductor industry. In the future, this study can be improved by continually integrating information on CFP from upstream to downstream companies in the semiconductor industry. Moreover, other environmental footprints should be considered, such as water footprint.

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